REMARKS

Claims 1, 3, and 5-16 remain in the application and stand rejected. Reconsideration of the rejection is respectfully requested in light of the following reasons.

Claims 1, 3, 5-7, 9-16 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,571,661 to Hoshino ("Hoshino"). The rejection is respectfully traversed.

Claim 1 is patentable over Hoshino at least for reciting: "forming a first protective layer over a gate, source, and drain of the transistor." As an example, FIG. 10 of the specification shows a protective oxide layer 104 over the transistor 100, which comprises a gate 98 and source-drains 96. FIG. 10 of the specification is reproduced below for ease of discussion. Such a protective layer allows separation of front end and backend processing of the integrated device, which is especially beneficial to the manufacture of capacitive micromachined ultrasonic transducers (CMUTs), for example. Among other advantages, embodiments of the invention allow for high temperature processing of CMUTs and other MEMS-based devices.

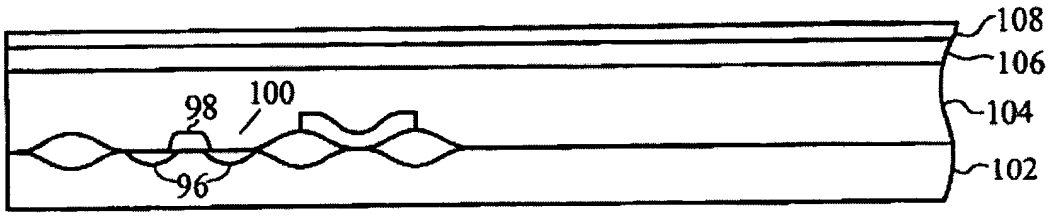
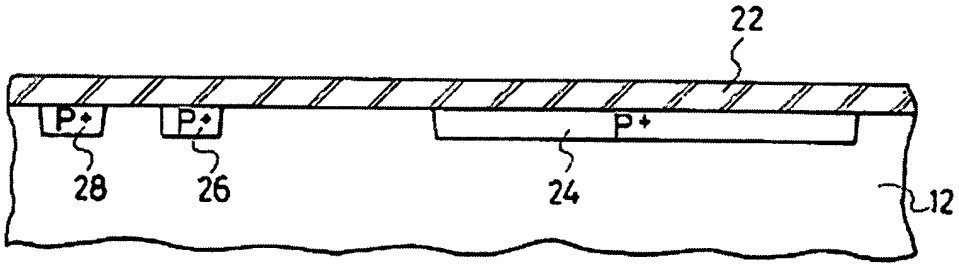


Fig. 10

In contrast, Hoshino does not teach or suggest forming a protective layer over a transistor and then forming a MEMS structure over the protective layer. In Hoshino, the oxide layer 22 cannot be the recited first protective layer because it is not formed over a transistor. This is now explained in connection with Hoshino FIG. 2A, which is reproduced below.

FIG. 2A



As shown in Hoshino FIG. 2A, the oxide layer 22 is formed over P+ regions 28 and 26 before they become part of a completed transistor. Note that P+ regions alone do not make a ***transistor***. The transistor including P+ regions 26 and 28 is not formed until after the gate 36 is formed in step FIG. 2D of Hoshino. This prevents the oxide layer 22 from protecting the transistor during fabrication of other subsequently formed layers. While this may be adequate for Hoshino's device, this limits fabrication of other devices as subsequently formed processing steps may degrade the transistor.

To expedite prosecution, claim 1 has been amended to recite that the protective layer is formed over the gate, source, and drain of the transistor. Clearly, Hoshino's oxide layer 22 is not formed over the gate 36. Note that this amendment is already implicit in claim 1 prior to the amendment as it already recited forming the first protective layer over the transistor, and active regions alone do not make a transistor. Therefore, it is respectfully submitted that claim 1 is patentable over Hoshino.

Claims 3 and 5-8 depend on claim 1, and are thus patentable over Hoshino at least for the same reasons that claim 1 is patentable.

Similar to claim 1, claim 9 is patentable over Hoshino at least for reciting: "forming a protective layer over the plurality of transistors ***after the plurality of transistors is formed***." As explained above, Hoshino does not teach or suggest forming a protective layer over a formed transistor.

Claims 10-16 depend on claim 9, and are thus patentable over Hoshino at least for the same reasons that claim 1 is patentable.

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Hoshino as applied to claims 1, 3, 5-7, and 9-16, and further in view of U.S. Patent No. 6,430,109 to Khuri-Yakub et al. ("Khuri-Yakub"). The patentability of claim 1 over Hoshino has already been explained above. Khuri-Yakub does not cure the deficiencies of Hoshino in regard to claim 1. Claim 8 depends on claim 1, and is thus patentable over Hoshino and Khuri-Yakub at least for the same reasons that claim 1 is patentable.

For at least the above reasons, it is believed that claim 1, 3, and 5-16 are in condition for allowance. The Examiner is invited to call the undersigned at (408)436-2112 for any question.

Respectfully submitted,
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